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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,984	02/04/2002	Tse-Yu Yeh	5580-04403	4187

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EXAMINER	
BUEHL, BRETT J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,984	YEH ET AL.	
	Examiner	Art Unit	
	Brett J Buehl	2183	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/4/02, 5/9/02, 11/18/02, 10/16/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/9/02, 11/18/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration and Fees as received on 2/4/02, IDS as received on 5/9/02, IDS as received on 11/18/02, and Change in Power of Attorney as received on 10/16/03.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 6, 7, 9-10, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 6 recites the limitation "wherein the second number of stages is dependent on whether the second instruction is one of the short floating point instructions, the floating point

multiply-add instruction, or one of the long-latency floating point instruction". This limitation is indefinite since it could be taken to mean the physical number of stages, which would indicate the physical number of stages can change, or time units the instruction spends in the stages. For purposes of examination, the examiner will interpret this limitation to indicate the number of time units the instruction spends in the stages.

8. Claim 7 is rejected for depending from claim 6.

9. Claim 9 recites the limitation "the indications in the scoreboard" in line 21. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 10 is rejected for depending from claim 9.

11. Claim 16 is rejected for the same reason as claim 6, see above.

Claim Rejections – 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1, 3-6, 8, 11, 13-15, 17 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Halfhill, "SiByte Reveals 64-Bit Core for NPUs". Johnson is used to further explain the functionality of Halfhill. Halfhill was cited in applicant's IDS filed on 5/9/2002.

14. Regarding claim 1, Halfhill has taught a processor comprising:

a. A first pipeline including a first stage at which instruction results are committed to architected state [ALU Pipelines, Register Writeback stage], wherein the first stage is separated from an issue stage of the first pipeline by a first number of stages;

b. A second pipeline [Floating Point Pipeline, page 46] including a second stage [Floating Point Pipeline, execution stage 4, page 46] at which an exception is reportable, wherein the second stage is separated from the issue stage of the second pipeline by a second number of stages which is greater than the first number [the number of stages between the issue stage and execution stage 4 is greater than the number of stages between the issue stage and the writeback stage of the integer pipeline]. [Halfhill states that his processor "supports single and double precision IEEE 754 floating point operations" (page 46). This means that there must be a stage at which exceptions are reportable before the instruction retires but after the instruction finishes execution (e.g. register writeback, or any of the execution stages) since the IEEE 754 standard requires floating point exception handling]; and

c. A control circuit configured to inhibit co-issuance of a first instruction to the first pipeline and a second instruction to the second pipeline if the first instruction is subsequent to the second instruction in program order [The processor of Halfhill is "strictly an in-order machine" [page 46, 2nd column], which means that the instructions must remain in-order from issue to completion. That would mean the issue logic has the ability to inhibit co-issuance of two instructions if the second instruction in program order depends on the first instruction in program order].

15. Regarding claim 3, Halfhill has taught the processor as recited in claim 1 wherein the second instruction is a floating point instruction ["It can issue two integer or two floating-point instructions in parallel with two load/store instructions on every clock cycle", page 46] and the second pipeline is a floating point pipeline [Floating-Point Pipeline, page 46].

16. Regarding claim 4, Halfhill has taught the processor as recited in claim 3 wherein the first instruction is an integer instruction ["It can issue two integer or two floating-point instructions in parallel with two load/store instructions on every clock cycle", page 46] and the first pipeline is an integer pipeline [Integer Pipeline, page 46].

17. Regarding claim 5, Halfhill has taught the processor as recited in claim 3 wherein the first instruction is a load/store instruction ["It can issue two integer or two floating-point instructions in parallel with two load/store instructions on every clock cycle", page 46] and the first pipeline is a load/store pipeline [Load/Store Pipeline, page 46].

18. Regarding claim 6, Halfhill has taught the processor as recited in claim 3 wherein floating point instructions include short floating point instructions (single precision, page 46, paragraph 1), a floating point multiply-add instruction (page 46, paragraph 2), and long floating point instructions (double precision, page 46, paragraph 1). It is inherent that the "short", or single precision, instructions take the shortest amount of time to execute since they work with the least amount of data (one operation on half the precision of the long instructions). It is also inherent that the multiply-add instructions take longer than the "short" floating point instructions since they do a normal floating point multiply followed by an add operation (similar to executing two floating point instructions). Finally, it is inherent that the "long", or double precision, instructions take the longest amount of time to execute due the double precision (twice as much

data to work with). Given that the number of stages required to complete the various instructions depends on the amount of work to be completed (i.e. a long-latency instruction, such as a divide, requires more time than an add instruction), it is inherent that an exception could be reported earlier for instructions requiring less work and less precision, meaning the second number of stages depends on the type of floating point instruction.

19. Regarding claim 8, Halfhill has taught the processor as recited in claim 1 wherein the control circuit is further configured to inhibit subsequent issue of instructions until a predetermined number of clock cycles prior to the second instruction reaching the second stage. Halfhill states that the processor described is a "strictly in-order machine" [page 46, 2nd column], which means it issues and completes instructions in-order. Johnson, used here to further explains what in-order issue with in-order completion means, states that "instruction issuing stalls when there is a conflict for a functional unit (the conflicting instructions are issued in series) or when a functional unit requires more than one cycle to generate a result" [page 18]. Since floating point instructions require more than one clock cycle to generate a result, it is inherent that the control unit must wait a predetermined number of clock cycles before issuing other instructions.

20. Regarding claim 11, given the similarities between the claims, the arguments as stated for claim 1 are applicable.

21. Regarding claim 13, given the similarities between the claims, the arguments as stated for claim 3 are applicable.

22. Regarding claim 14, given the similarities between the claims, the arguments as stated for claim 4 are applicable.

23. Regarding claim 15, given the similarities between the claims, the arguments as stated for claim 5 are applicable.

24. Regarding claim 17, given the similarities between the claims, the arguments as stated for claims 8 are applicable.

25. Regarding claim 20, it is inherent that there be a carrier medium for the processor to function, therefore, the arguments as stated for claim 1 are applicable to claim 20.

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 2, 7, 9-10, 12, 16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halfhill, in view of the IEEE Floating Point Standard.

28. Regarding claim 2, Halfhill has taught the processor as recited in claim 1, but has not explicitly taught wherein the control circuit is configured to selectively inhibit co-issuance of the first instruction and the second instruction responsive to whether or not the exceptions are enabled for the second instruction.

29. However, the examiner takes OFFICIAL NOTICE that if the floating point exceptions are disabled, which is allowed by the IEEE 754 floating point standard and followed by Halfhill (page 46), the instruction cannot cause an exception and, therefore, does not affect the precise state of the machine. This means that a floating point instruction with exceptions disabled can be

co-issued with another instruction, since the floating point instruction cannot cause an exception, therefore still allowing for a precise machine state. Therefore, it would have been obvious to one of ordinary skill in the art to co-issue a first instruction with a second instruction if the exceptions are disabled for the second instruction since it would still allow for a precise machine state

30. Given the similarities between the claims, the arguments as stated for claim 2 are also applicable to claim 12.

31. Regarding claim 7, Halfhill has taught the processor as recited in claim 6, but has not explicitly taught wherein if the second instruction is not one of the short floating point instructions, the control circuit is configured to inhibit co-issuance of subsequent floating-point instructions, in program order, to a third pipeline.

32. However, one of ordinary skill in the art would have recognized that if the second instruction is a FP multiply-add instruction, then a short FP instruction cannot be co-issued to the other FP pipeline since the short instruction would finish execution before the second instruction since the multiply-add instructions take longer to execute. Therefore, it would have been obvious to one of ordinary skill in the art that the control unit would not be able to co-issue a second floating point instruction if the first floating point instruction was not a short instruction since the multiply-add instructions and the long instructions take longer to execute and the co-issued instructions must finish at the same time.

33. Given the similarities between the claims, the arguments as stated for claims 6 and 7 also apply to claim 16.

34. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halfhill and further in view of Patterson.

35. Regarding claim 9, Halfhill has taught the processor as recited in claim 8, but has not explicitly taught a scoreboard coupled to the control circuit, wherein the control circuit is configured to logically combine the indications in the scoreboard, and wherein the control circuit is configured to permit subsequent issue of instructions responsive to the logical combination having a result indicating that no register writes are pending.

36. However, Patterson has taught a scoreboard scheme in a superscalar processor to track the data dependencies between instructions in a processor [page 242] since "if two instructions are data dependent they cannot execute simultaneously or be completely overlapped" [page 230]. Although the processor in Halfhill does not allow for out-of-order execution, the scoreboard would allow the tracking of register writes, allowing for the data dependencies to be tracked. Inhibiting instruction issuing when there are register writes ensures correct instruction execution since there is no chance a depending instruction will read the a register before it is written. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor of Halfhill to include a scoreboard for tracking register writes, allowing for the tracking of data dependencies and ensuring proper execution of the instructions.

37. Given the similarities between the claims, the arguments as stated for claim 9 are also applicable to claim 18.

38. Regarding claim 10, Halfhill further in view of Patterson has taught the processor as recited in claim 9 but has not explicitly taught wherein the scoreboard comprises a bit for each register indicative, when set, that a write is pending to the register, and wherein the logical

combination of the bits is a logical OR, and wherein the control circuit is configured to permit subsequent issue of instructions responsive to the logical OR being zero.

39. However, one of ordinary skill in the art would have recognized that only a bit is required for each register to indicate a pending write since there is no register renaming, which would require additional information to be stored in the scoreboard. In order to stall any depending instructions from issuing due to the pending write, it would have been obvious to logically OR each indicator bit because a logical OR combines a set of binary values such that any affirmative value set results in an affirmative output Because any pending register write would block issuance, using a logical OR provides for any one or more set scoreboard bit within the set to indicate that issuance should be blocked. Therefore, it would have been obvious to one of ordinary skill in the art to indicate a pending register write with a bit for each register and to logically OR the indicators together to determine if there are pending register writes, not issuing instructions if there is a pending write.

40. Given the similarities between the claims, the arguments as stated for claim 10 are also applicable to claim 19.

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of art disclosed by the references cited and the objections made. Applicant must show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

42. Inquiries concerning this communication or earlier communications from the examiner should be directed to Brett J. Buehl who can be reached at (703) 305-4663 or <brett.buehl@uspto.gov>. The examiner can normally be reached between the hours 8:00am – 5:30pm (EST), Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan, can be reached at (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

43. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RICHARD L. ELLIS
PRIMARY EXAMINER